Remarks

Drawings Specification

A substitute specification conforming the application text to US style and practice is submitted herewith. The substitute specification does not add new matter.

On amended page 6 of the description the reference sign 27 denoting the buffer has been corrected.

Regarding the other reference signs 22 - 25, 28 - 30, these signs are mentioned in the description of Fig. 2 and included in this figure. Thus, a correction of the drawings does not appear to be necessary.

The abstract of the disclosure is amended to place all sentences into a single paragraph, i.e., to remove the line break between sentences 2 and 3.

On page 2, the specification is amended to specify that the cited state of the art is a German patent application.

Claim Objections

The Examiner appears not to have seen our Preliminary Amendment, which avoided multiple dependencies in the claims. But his treatment of the dependencies appears applicable.

Claims 16 and 17 are amended to substitute "the system" for "the function".

Claim Rejections – 35 USC 102 (b)

Claims 1-4, 6-7, 9, 12-21 and 23 stand rejected as being anticipated by Eastvold et al.

Valid rejection under 35 USC 102 requires that each feature of a rejected claim be disclosed in a single reference. "For anticipation under 35 USC 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present." MPEP 706.02(a)

Eastvold et al does not disclose each feature of the rejected claims.

The network as shown in Fig. 1 of Eastvold et al. is not entirely ring-shaped. Although the DTU's are connected via a ring shaped serial connection, this does not hold for the system monitor 16 which is merely connected to master DTU 34. In contrast thereto, all devices as defined in claim 1 <u>are part of the ring shaped network</u>.

Furthermore, Eastvold et al. fails to teach that temporarily stored data are monitored by a checking logic of a peripheral safety-related unit in such a manner that, in the case of a fault, a safe state of the output unit (10) for the control process is initiated. Suppressing data cannot be compared to an initiation of a safe state. The latter necessarily implies a <u>change of the state</u> of the safety related unit. If, on the other hand, data destined for one of the DTUs are merely suppressed, as taught in Eastvold et al., the state of the respective DTU <u>does not change at all</u>.

Moreover, claim 1 defines a control unit and a peripheral monitoring unit. As the monitoring unit is definitely <u>peripheral</u>, both units are distinct devices and cannot be compared with a combination of master DTU 34 and system monitor box 16 as disclosed in Eastvold et al.

As well, there is no hint for a person skilled in the art to modify the system as disclosed in Eastvold et al. so as to derive a system according to claim 1, which comprises means for initiating a safe state of the output unit for the control process in the case of a fault.

<u>Claim Rejections – 25 USC 103 (a)</u>

Claims 5 and 22 stand rejected as being unpatentable over Eastvold et al in view of Dawson.

Claims 8, 10-11 and 24 stand rejected as being unpatentable over Eastvold et al in view of Cawley.

MPEP 2142 sets forth "The Legal Concept of *Prima Facie* Obviousness."

To establish a *prima facie* case of obviousness under 35 USC 103(a) the initial burden is on the Examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references."

MPEP 2143 sets forth basic requirements of a *Prima Facie* case of obviousness.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck,* 947 F.2d 488. 20 USPQ2d 1438 (Fed. Cir. 1991)."

The cited references do not motivate or suggest to a skilled artisan to combine these references to produce applicant's invention as claimed.

Dawson does not teach redundant input channels as defined in claim 22. According to the circuit diagram as depicted in Fig. 10 of Dawson, two units 330, 340 read data from input lines 212, 312. However, claim 22 defines that the device comprises two bus units (22, 23), <u>to forward the output data of a bus unit (22) also to the input section of the other bus unit</u> (23) in order to be able to fetch information from the control process via redundant input channels (24, 25) and in

order to provide the output data of a peripheral monitoring unit (4) for read-back. However, the output lines 310, 315 of the units 330, 340 are only connected with comparator 320. Undoubtedly, therefore, none of the output lines 310, 315 of the units 330, 340 is connected to the input of the other unit.

As Dawson does not teach this feature of two bus units connected so as to forward output data of one unit to the input of another unit, the subject matter of claim 22 therefore cannot be rendered obvious over a combination of Eastvold et al. and Dawson.

As dependent claims 2 - 21, 23 and 24 incorporate all features of claims 1 and claim 22, respectively, the subject matter of these claims is new and inventive, too.

Moreover, claim 3 defines that the data which are temporarily stored in the peripheral safety-related unit are read back by a bus unit of the peripheral safety-related unit. However, Eastvold et al. does not disclose a similar feature. Particularly, the passages of Eastvold er al. cited in the Office Action with respect to claim 3 merely disclose that data are subsequently sent from one DTU to the next DTU within the network. This, however, does not mean that data which are stored in a bus unit are read back by the same unit, as would follow from a system according to claim 3.

As well, claim 4 defines an assembly similar to claim 3. Although the DTUs as disclosed in Eastvold et al. may have a buffer, it is not disclosed therein that the content of the buffer is read back by the bus unit 23 whereby both the buffer and the bus unit 23 are components of the peripheral safety-related unit. The passages of Eastvold et al. cited in the Office Action merely disclose that a CRC is performed with data received from another DTU.

Further, col. 11, lines 45-63 of Eastvold et al. neither discloses nor implies that data of an SPC are overwritten by a peripheral monitoring unit. This passage merely discloses that

performance and history information is stored in a system monitor database.

Regarding claim 8, Cawley merely teaches to insert a "BadPacket" indicator at the end of the packet. Consequently, Cawley just teaches to add data to existing data rather than manipulating the existing data. However, adding a flag which identifies a packet to contain bad data is different from manipulating the data, e.g., so as to correct the package content.

It is further submitted that a system according to claim 10 cannot be derived from a combination of the teachings of Eastvold et al. and Cawley. Regarding the overwriting of faulty data, Cawley just describes the opposit of what is defined in claim 10. Cawley teaches (see col. 9, lines 4 - 21) that a data packet transmitted by a router is not allowed to be overwritten, if the receiving router detects a CRC-fault. Data in the FIFO ring buffer are only overwritten if the data package has arrived at the receiving router without CRC faults. If data have been transmitted correctly, i.e. after agreement, then the data in the FIFO of the transmitting router are overwritten. In contrast thereto, claim 10 defines that data are overwritten to prevent agreement.

Moreover, it is not disclosed in Eastvold et al. that the peripheral safety-related unit only becomes active if it has received an agreement for the data of the output unit via the checking unit as defined in claim 12. Eastvold et al., specifically col. 15, lines 35 - 39 merely discloses that packages with valid CRC and "Broadcast" data packets are accepted, whereas other packets are dropped. In contrast to the opinion expressed in the Office Action, it is not disclosed that the dropping prevents further processing.

As well, we are unable to share the view expressed with respect to claim 14. The passage which is cited as relevant for the subject matter of claim 14 (col. 6, lines 1-2) refers to the DTUs 12 but not to master DTU 34. Furthermore, it is not disclosed that any of the DTUs performs control functions like the system monitor box 16.

Furthermore, we cannot agree with the view expressed with respect to claim 19. Again, with reference to the discussion of claim 1, the control unit and peripheral monitoring unit cannot be compared with a combination of the system monitor box 16 and master DTU 34 according to Eastvold et al.

Regarding claim 21, the same arguments as put forward with respect to the feature of initiating a safe state according to claim 1 are valid. Dropping data packets does not change the state of a DTU 12 or 34 at all.

Wherefore further consideration and allowance of the application as amended is respectfully requested.

A two-month extension of time in which to respond to the outstanding Office Action is hereby requested. PTO-2038 is enclosed authorizing credit card payment in the amount of $450 is enclosed for the prescribed Large Entity two-month extension fee.

Respectfully submitted,

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I hereby certify this correspondence is being submitted to Commissioner for Patents, Washington, D.C. 20231 by facsimile transmission on May 12, 2005, fax number (571) 273-3657.

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Substitute Specification

Circuit Arrangement for Protected Data Transmission, Particularly in Ring-Shaped Bus Systems

Cross-Reference to Related Applications – Not Applicable

Statement Regarding Federally Sponsored Research & Development – Not Applicable.

Background of the Invention

Field of the Invention

~~Description~~

[0001] The invention relates to a circuit arrangement for protected data transmission, particularly in ring-shaped bus systems.

Description of Relevant Art

[0002] In machine and plant construction today, movements and processes are not infrequently controlled which represent a danger to the life and health of persons, particularly the operating personnel, in the case of a fault or if they fail. Apart from these dangers, however, valuable machine parts must also be protected which can suffer great financial damage in the case of possible malfunctions.

[0003] Any faults which may occur must, therefore, be recognized by the process or the existing control facilities and the machine should always be driven in a state which can be considered safe. As a rule, redundant structures are necessary for this which monitor the safety functions independently of the actual control. In machine or plant construction, detection of a single error is frequently sufficient for fault detection. After this fault has been detected, the control process can then be interrupted and stay in a safe state. This prevents any damage by faulty continuation of the process.

[0004] The methods for fault detection and the measures necessary for these are stated in

international standards DIN V VDE 0801 and DIN ISO 61508. By means of the principles given in these standards, the manufacturers of automation equipment have developed in recent years different strategies which allow safe transmissions on bus systems, see, for example, the "profibus with F-Profil, PNO and safety-bus P by Pilz and Sick.

[0005] In addition, control systems will reach the market which already have internally redundant structures and thus, in interplay with said safe bus systems, allow fault detection; see, for example, the bus systems from Siemens, particularly the equipment series S 7 400 F, or the PSS 3000 series by Pilz.

[0006] However, the methods implemented there can only be used with completely new installation of the necessary components and protect only inadequately against systematic faults.

Brief Summary of the Invention

[0007] Instead, the invention has the object of detecting faults in a process which is only built up with standard units.

[0008] In addition, it should preferably be not only any faults occurring in the transport of data via a bus system used, but also disturbances or programming errors in the control device which are detected and eliminated.

[0009] The circuit arrangement thus represents an implementation of a method which has already been filed under the post-published German patent application no. 198 57 683.8, the full extent of the content of which is also made the subject matter of the present patent application by reference.

[0010] The method is particularly suitable for all ring-shaped bus systems, the technology described being optimally adapted for the interbus standard. In this case, a requirement

profile was already worked out at the beginning of 1999 and then published, IEE journal, April 1999, Karsten Meyer-Gräfe: "Interbus goes Safety".

Brief Description of the Drawings

[0011] In the text which follows, the invention is described in more detail, referring to preferred embodiments and the attached drawings, in which:

[0012] Fig. 1 shows the configuration for a first embodiment of a system for protected data transmission,

[0013] Fig. 2 shows the internal configuration of the peripheral safety-related unit of the system for protected data transmission.

Detailed Description of the Invention

[0014] In the text which follows, the invention will be described in greater detail, initially by referring to Fig. 1. Fig. 1 shows a suitable configuration for such a system.

[0015] The control unit (1) handles all control functions in the process as is known, for example, from the conventional interbus system. The control unit (1) also detects possible faults and can interrupt processes or bring them to a safe state.

[0016] In the case of its own failure or in the case of faulty data transport, however, the control unit (1) is conventionally not able to produce the desired safe state. This failure also occurs, for example, if there is extensive separation between process control and safety control in the control system. Since there is conventionally no redundancy here, either, an undetected fault may have grave consequences.

[0017] According to the invention, other components are added which detect and eliminate a possible fault. These units are: a peripheral monitoring unit (4) and one or more peripheral safety-related units (9) in the process, which are only necessary where safety-related data are

received or transmitted.

[0018] The control unit (1) contains a data map register (2) which sends all output data and other checking signals via the data line (13) to the peripheral units (7, 8, 12, peripheral safety-related unit 9 and peripheral monitoring unit 4).

[0019] Since the bus transport works in a similar way to a shift register, all peripheral units send their input data to the control unit in the same bus cycle via the return line (14) and these data are available in the data map register (3). In a subsequent SPC (stored-program control) cycle, the SPC then processes the data from its two map registers (2, 3) and thus generates the necessary state for the process.

[0020] Without the peripheral monitoring unit (4) and the peripheral safety-related unit (9), however, the SPC is not capable of controlling a programming error, a state due to disturbance or failure or a data error due to the wrong bus transport. The peripheral monitoring unit (4), therefore, contains its own microprocessor which monitors the transmitted data of the SPC and only examines the safety-related quantities for appropriateness, particularly their correctness.

[0021] Thus, the peripheral monitoring unit (4) with the transfer unit (5) is capable of monitoring the SPC. However, the peripheral monitoring unit (4) can also additionally read the data of the inputs of the peripheral units via the transfer unit (6) installed in the return path. Since the peripheral safety-related unit (9) also forwards its output information (D3) directly to the input section of the bus unit (23), it is possible to check directly whether the bus transfer has worked correctly.

[0022] Furthermore, the peripheral monitoring unit (4) with its transfer unit (5) is also capable of manipulating the data for the peripheral safety-related unit (9). In particular, the peripheral

monitoring unit (4) can overwrite data of the SPC and thus prevent agreement with the data output from the peripheral safety-related unit (9). The peripheral safety-related unit (9) becomes active only if it has received an agreement for the data of the output unit (10) via the checking unit (11).

[0023] The timing with the data transport is shown in the following table:

SH	MT	ST		1		2		D3		C3		4		SR		MR
		A	E	A	E	A	E	A	E	A	E	A	E	A	E	
0	LBW		ST		E1		E2		E3		EC3		E4		ESR	
1	ASR	LBW	LBw	ST	ST	E1	E1	E2	E2	E3	E3	EC3	EC3	E4	E4	ESR
2	A4	ASR	ASR	LBW	LBW	ST	ST	E1	E1	E2	E2	E3	E3	EC3	EC3	E4
3	1	A4	A4	ASR	ASR	LBW	LBW	ST	ST	E1	E1	E2	E2	E3	E3	EC3
4	A3	1	AC3	A4	A4	ASR	ASR	LBW	LBW	ST	ST	E1	E1	E2	E2	E3
5	A2	A3	A3	AC3	AC3	A4	A4	ASR	ASR	LBW	LBW	ST	ST	E1	E1	E2
6	A1	A2	A2	A3	A3	AC3	AC3	A4	A4	ASR	ASR	LBW	LBW	ST	ST	E1
7	ST	A1	A1	A2	A2	A3	A3	AC3	AC3	A4	A4	ASR	ASR	LBW	LBW	ST
8		ST	ST	A1	A1	A2	A2	A3	A3	AC3	AC3	A4	A4	ASR	ASR	LBW

[0024] The timing diagram shows the state after each shift information in the ring by means of a

preferred example, the Interbus system by Phoenix Contact GmbH and Co. KG.

[0025] The information AC3 can be manipulated by the peripheral monitoring unit (4) with the transfer unit (5) and can be overwritten. The peripheral safety-related unit (9) thus receives in its checking logic (11) an additional information item which prevents a faulty output.

[0026] As can also be seen from the timing diagram, the peripheral monitoring unit (4) can also read the data of the output from the peripheral safety-related unit (9) (EC3). These data represent the direct output information of the peripheral safety-related unit (9) so that a bus error is reliably detected.

[0027] The internal configuration of the peripheral safety-related unit (9) is shown in figure 2.

[0028] The peripheral safety-related unit (9) consists of two bus units (22, 23) so that input information can be fetched redundantly (24, 25). In addition, the output information Dn from a bus unit (22) is mapped via the input section of the other bus unit (23). A possible error in the internal storage or during the bus transport is thus detected in the subsequent cycle of the bus transport. The output information Dn is written into the buffer [[(7)]] (27) by the control unit (SPC).

[0029] However, the checking logic (11) additionally decides whether the information of the buffer [[(7)]] (27) appears at the peripheral unit via the output logic (28). This checking logic (11) can either release the stored information via the line (30) or delete the state via the line (31) so that the output (29) brings the control process into a safe state.

[0030] In principle, however, the circuit arrangement operates in many areas just like a normal decentralized SPC system. The components merely additionally allow inputs to be redundantly monitored and stored output information to be examined for appropriateness, particularly freedom from faults before it is output. Furthermore, the monitoring unit can also

detect faults which have not only been produced by failure or disturbance but were caused by an error in programming or parameterizing.

[0031] The present circuit arrangement thus allows data which are necessary for configuring fault-tolerant structures to be transmitted on standard ring-shaped bus systems.

[0032] To implement the invention, a monitoring unit and peripheral input and output units transmitting or receiving data for control purposes are used.

[0033] The circuit arrangement handles the task of detecting any faults which can become a danger for the control process, particularly for the transmission of control, sensor or actuator data, within a machine or plant. Due to its internal configuration, the circuit arrangement identifies a possible error even before the error is transmitted to the control process and initiates a protected switch-off. In this arrangement, it is of no importance whether it is the external control unit or the bus system used which is responsible for the error.

Abstract (Amended)

The present circuit arrangement allows data, which are necessary for building up fault-tolerant structures, to be transmitted on standard ring-shaped bus systems. Its implementation requires a monitoring unit and input and output units which transmit or receive data for control. The circuit arrangement handles the task of detecting any faults which can become a danger for the process within a machine or plant. Due to its internal configuration, the circuit arrangement identifies any fault even before the detection of the fault and initiates a protected switch-off. In this arrangement, it is of no importance whether it is the external control unit or the bus system used which is responsible for the fault.

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